indicated to Applicants as being overcome during the January 14, 2002 telephone conference with the Examiner.

B. Rejection of Claims 1-3

The Applicants traverse this ground of rejection for the reasons set forth below. The present invention is directed to a circuit and corresponding method for generating an optimal initial rasterization starting point estimate for a rasterizer (e.g. raster engine) to use when rendering an image. The initial rasterization starting point can be used to efficiently and quickly render a primitive by providing an appropriate raster engine with an initial scanning point that is substantially within or near the primitive. By employing the circuit and method of the present invention, the time for scanning and rendering a primitive is significantly shorter as compared to conventional methods. The inventive method which provide such advantages includes the steps of:

> "...generating region bits representing a location each of the first, second and third vertices with respect to a tile being rendered;
> generating coordinate data representing an initial rasterization starting point estimate based in part on the region bits..."

The resulting region bits define whether the triangle, or other suitable primitive, lies within a given pixel currently being rendered. As claimed, the initial rasterization point is "...based in part on the region bits..." Thus, the initial rasterization starting point lies within or substantially near the location defined by the region bits. Such combination of steps and the benefits provided thereby are not taught or suggested by the combination of references as cited by the Examiner.

As understood, Aleksic is directed to a pixel scanning method used when a portion of an object being scanned crosses, or lies outside of a page boundary. The scanning of the object is described, for example, at col. 3, line 62-col. 4, line 10 (walk along each span, incrementing and x-coordinate of pixels along the span and decrementing the number of pixels making up the span). However, Aleksic is silent on how the initial scan point is generated. As Aleksic does not disclose how the initial rasterization starting point is generated, it does not teach or suggest "...generating coordinate data representing an initial rasterization starting point estimate based in part on the region bits..." as defined in claim 1.

In addition, adding the teachings of Lentz, et al. to the teachings of Aleksic will also not render the invention as defined in claim 1 obvious as Lentz, et al. does not overcome the aforementioned deficiency in Aleksic. In addition, Lentz, et al. also does not teach or suggest

"...generating coordinate data representing an initial rasterization starting point estimate based in part on the region bits..." as defined in claim 1. As understood, Lentz, et al. is directed to a system and corresponding method for rendering polygons that incorporate a w-bit wide render mask to provide an indication of which bits along a scan line are to be subsequently rendered. *See*, for example, col. 6, lines 34-55. However, there is no teaching or suggestion of the generation or use of an "...initial rasterization starting point..." data as defined in claim 1. In fact, Lentz, et al. expressly states that "methods for determining the order of traversal are not discussed here." (*See*, col. 9, lines 52-53). Thus, the initial point at which to start rasterization is seemingly not a consideration in Lentz, et al. Accordingly, as Aleksic does not disclose the method of generating and "...initial rasterization starting point..." and Lentz, et al. explicitly does not discuss the generation of an initial rasterization starting point (*see*, col. 9, lines 52-53), the combination of Aleksic and Lentz, et al. does not render the claimed invention obvious.

To overcome the shortcomings of the combination of Aleksic and Lentz, et al., the Examiner in the instant Office Action has added the teachings of Wong, et al. to the combined teachings of Aleksic and Lentz, et al. and states that the combination thereof renders the claimed invention obvious. The Applicants traverse this ground of rejection and the addition of the Wong, et al. reference for the reasons set forth below. As understood, Wong, et al. is directed to a scanning methodology where scan direction is selected based on a determination of major and minor axes (*see*, for example, col. 4, lines 20-23). The scan axes are selected in response to an edge function, which determines whether a polygon to be rendered lies within a given tile (*see*, for example, col. 6, lines 13-67). Based on the results of the edge function, the resulting polygon is classified into one of several groupings (*see*, for example, FIG. 9-10 and col. 5, lines 31-44) and uses the resulting group value as an index to a look-up table (LUT), which provides the initial sampling point (*see*, for example, col. 5, lines 45-50). Thus, the location at which a raster engine initially scans, as disclosed in Wong, et al., is not based on generated "...region bits..." as defined in claim 1, but rather on a value contained in a LUT. In using the aforementioned method, the initial starting point will be located at one of the corners of the tile (*see*, for example, col. 5, lines 49-52), not within or substantially near the primitive to be rendered as defined in claim 1. Thus, Wong, et al. also does not teach or suggest the invention as defined in claim 1.

Consequently, as neither the combination of Aleksic and Lentz, et al. or Wong, et al. individually teach or suggest the invention as defined in claim 1 or provide a motivation to

combine the same, their combination cannot and does not render the invention as defined in claim 1 obvious. Accordingly, reconsideration of the rejection of claim 1 is respectfully requested.

Claims 2-3 directly or indirectly depend upon and include all the limitations of claim 1 and are allowable at least for the reasons associated with claim 1. Accordingly, reconsideration of the rejection of claims 1-3 is respectfully requested.

B. Rejection of Claims 4-6

On page 5, paragraph 2 of the Office Action, the Examiner has rejected claims 4-5 by stating that they "...are similar in scope to the claims 1 and 2, and thus the rejections of claims 1-2 hereinabove are also applicable to claims 4 and 5..." By making this rejection, the Examiner has completely ignored an entire limitation that is present in claim 4 that is not present in claim 1. More specifically, claim 4 includes a limitation directed to:

> "...the initial rasterization starting point estimation circuit including a circuit for discarding a triangle when the corresponding vertex data lies outside a boundary defined by the region bits..."

Thus, by the Examiner basing his rejection of claims 4 and 5 on his prior rejection and reasoning related to claim 1, the Examiner has not met his *prima facie* showing of obviousness under MPEP 2142 as claim 4 includes a limitation that is not directly or analogously present in claim 1, nor discussed in connection therewith. Consequently, the Applicants assert that the rejection of claim 4 is improper and should be withdrawn or, in the alternative, that claim 4 is allowable over the art of record and such action is earnestly solicited. If the Examiner disagrees with the assertions made above, or wants to substantiate and clarify his rejection to the aforementioned claims, the Applicants request that such action be made the part of a subsequent non-final Office Action.

Claims 5-6 directly or indirectly depend upon and include all the limitations of claim 4 and are allowable at least for the reasons associated with claim 4. Accordingly, reconsideration of the rejection of claims 4-6 is respectfully requested.

C. Rejection of Claims 7-17

(i) Claims 7-8

Claims 7-8 directly or indirectly depend upon and include all the limitations of claim 1 and are allowable at least for the reasons associated with claim 1. In addition, these claims define subject matter that is not taught or suggested by the combination of references as cited by the Examiner. More specifically, as discussed above, none of the cited references discloses operating on region bits which are defined, in part, based on sorted vertex information. Thus, the combination of references does not teach or suggest "...discarding triangles when the vertices correspond to locations outside the tile represented by the region bits..." as defined in claim 7, nor "...the initial rasterization starting point is defined by the intersection of the sorted vertices and the position represented by the region bits..." as defined in claim 8. Accordingly, reconsideration of the rejection of claims 7-8 is respectfully requested.

(ii) Claims 9-13

Claims 9-13 directly or indirectly depend upon and include all the limitations of claim 4 and are allowable at least for the reasons associated with claim 4. In addition, these claims define subject matter that is not taught or suggested by the combination of references as cited by the Examiner. More specifically, none of the aforementioned references either individually, or in combination teach or suggest "...the region bits define the top edge, bottom edge, right edge and left edge of the current tile being rendered..." as defined in claim 13. On page 7, paragraph 2, the Examiner cites FIG. 9-12 and col. 2, lines 5-25 of Wong, et al. as reciting the aforementioned limitations. The Applicants traverse this reason for rejection. As clearly illustrated in FIG. 9-12 and discussed, for example, at col. 5, lines 31-50 and col. 6, lines 14-67, the boundaries of the primitive (i.e. polygon) are defined by edge functions. No indication of region bits, or the boundaries thereby is disclosed in Wong, et al. Accordingly, reconsideration of the rejection of claims 9-13 is respectfully requested.

(iii) Claims 14-17

The Applicants traverse this grounds for rejection for the reasons set forth below. Claim 14 is an apparatus claim which defines a circuit which provides the initial rasterization starting point estimate according to the method of the present invention. As defined in claim 14, the circuit includes among other things:

"...a sorting circuit operative to provide sorted vertex data...in coordinate-dependent fashion, the vertex data including x-coordinate and y-coordinate position information;

a region calculation circuit...operative to generate region bits representing a position of the primitive with respect to a tile being rendered; and

initial rasterization starting point circuit including a discard circuit operative to discard the vertex data of a primitive that lies outside the boundary defined by the region bits..."

Such a combination of is not taught or suggested by the combination of references as cited by the Examiner. As discussed in greater detail above, Aleksic is silent on how the initial scan point is generated. Lentz, et al. does not discuss, or is concerned with how the initial scan point is discussed. Thus, the combination of Aleksic and Lentz, et al. does not render the first limitation of claim 14 obvious. In addition, Wong, et al. discloses that the initial rasterization starting point is based on information contained in an LUT as indexed by an edge function (*see*, for example, col. 6, lines 63-67), which does not depend upon, use or relate to region bits. A preliminary discussion of vertex data is disclosed, for example, at col. 7, lines 44-54; however, there is no disclosure within Wong, et al. as to whether such vertex information is "...sorted in a coordinate-dependent fashion..." or subsequently used as defined in claim 14. Thus, as none of the references cited by the Examiner teach or suggest sorting input vertex data in coordinate-dependent fashion and the subsequent use thereof, the Applicants submit that the combination of references does not teach or suggest this limitation of claim 14.

In addition, none of the aforementioned references teaches or suggests the use or operation of a "...discard circuit operative to discard the vertex data of a primitive that lies outside the boundaries defined by the region bits..." as defined in claim 14. More specifically, Aleksic and Lentz, et al. are silent on the use of a discard circuit. Wong, et al. does not disclose the use or operation of a discard circuit as the scanning of a primitive, or other suitable polygon, is started at the corner of a tile to be rendered (*see*, for example, col. 5, lines 49-50) and continues along both a major and a minor axes until the polygon to be rendered is located (*see*, for example, col. 7, lines 12-43). As such, because the scanning is defined as being performed within an entire tile, discarding is not performed. Consequently, as neither Aleksic, Lentz, et al. or Wong, et al. teaches or suggests the use or presence of a "...discard circuit operative to discard the vertex data of a primitive that lies outside the boundary defined by the region bits..."

as defined in claim 14, the combination of such references also does not render this limitation obvious.

Accordingly, as the combination of references as cited by the Examiner does not teach or suggest at least two limitations of claim 14, such combination of references cannot and does not render the invention as defined in claim 14 obvious. Accordingly, reconsideration of the rejection of claim 14 is respectfully requested.

Claims 15-17 directly or indirectly depend upon and include all the limitations of claim 14 and are allowable at least for the reasons associated with claim 14. Accordingly, reconsideration of the rejection of claims 14-17 is respectfully requested.

Based on the above amendments and remarks, the Applicants submit that claims 1-17 are now in proper condition for allowance and such action is earnestly solicited.

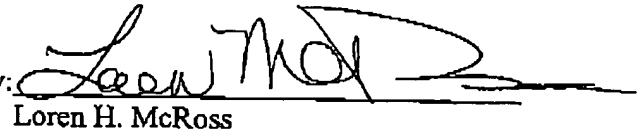
III. Change of Correspondence Address

Per the immediately preceding response and the January 14, 2002 teleconference, please address all future communications relating to the above-identified application to the following:

Christopher J. Reckamp, Esq.
VEDDER, PRICE, KAUFMAN & KAMMHOLZ
222 North LaSalle Street
Chicago, Illinois 60601

The Commissioner is hereby authorized to charge any underpayment or credit any overpayment to Deposit Account No. 50-0441 for any payment in connection with this communication, including any fees for extension of time, which may be required. The Examiner is invited to call the undersigned if such action might expedite the prosecution of this application.

Respectfully submitted,

By: 

Loren H. McRoss
Registration No. 40,427

Date: January 23, 2002

VEDDER, PRICE, KAUFMAN &
KAMMHOLZ
222 N. LaSalle Street
Chicago, IL 60601
(312) 609-7500
FAX: (312) 609-5005